

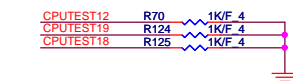
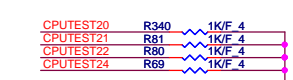
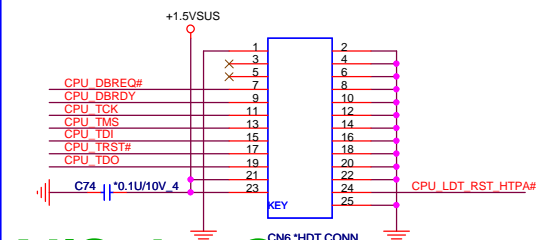
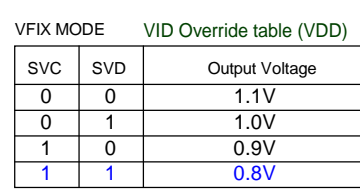
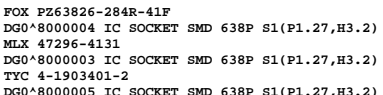


PV,delete all external clock GEN reserve material



**PROJECT : AX2/7**  
Quanta Computer Inc.

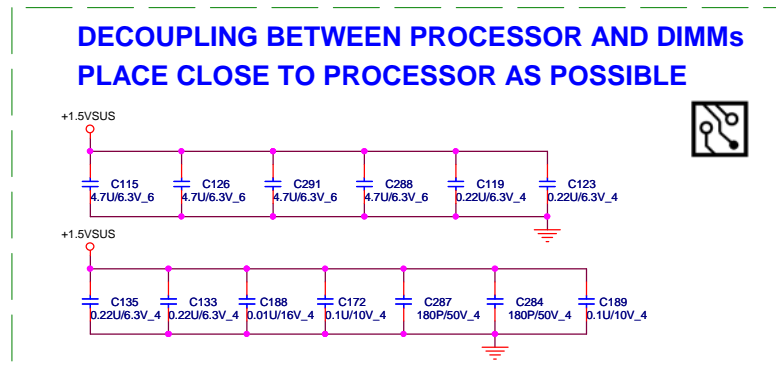
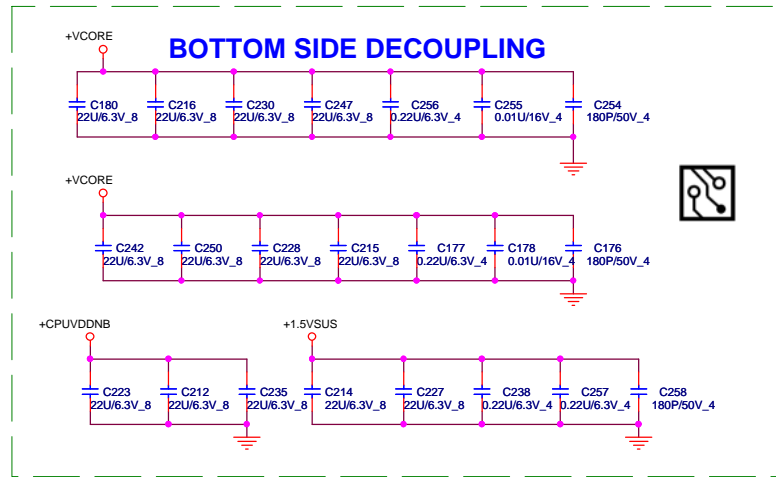
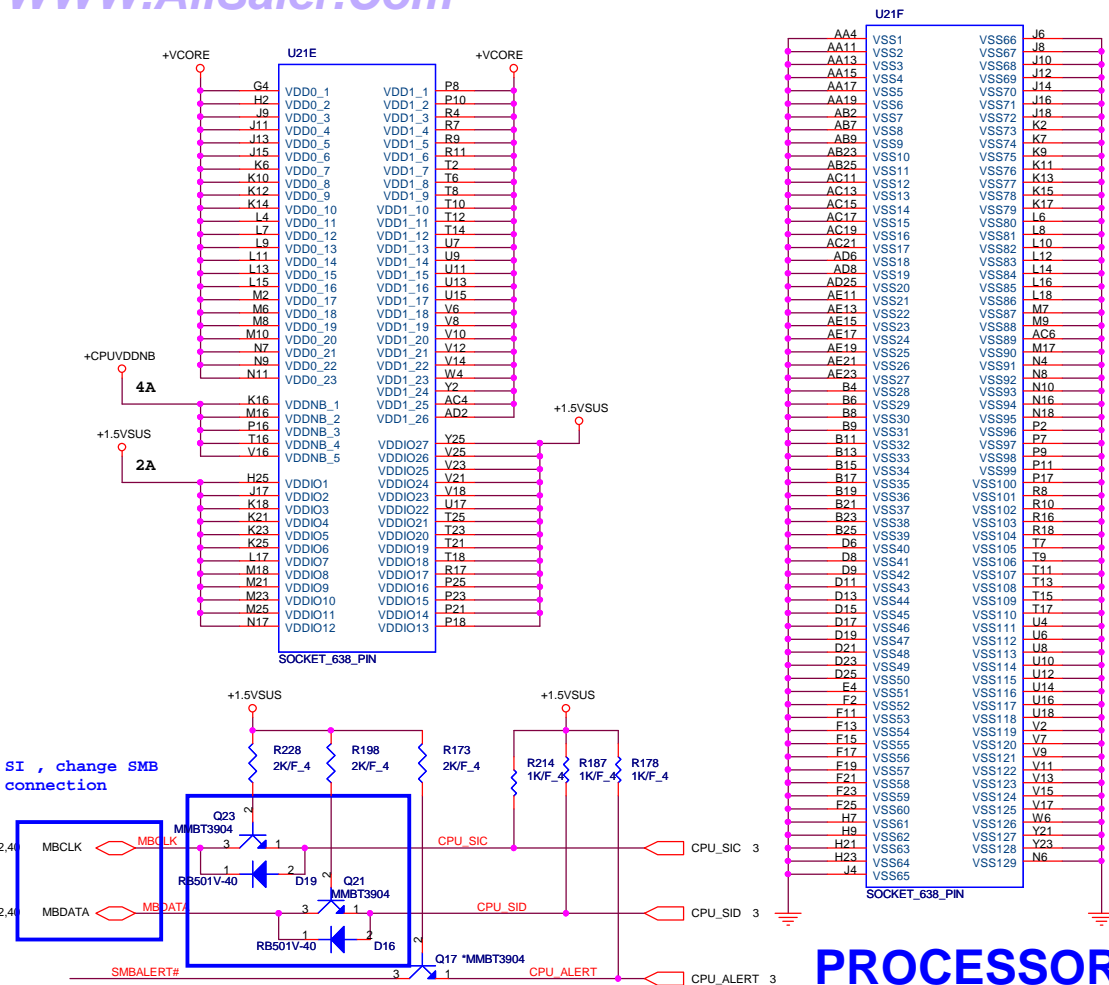
Size Custom	Document Number <b>Clock Generator</b>	Rev 1A
Date: Wednesday, December 23, 2009 Sheet 2 of 42		



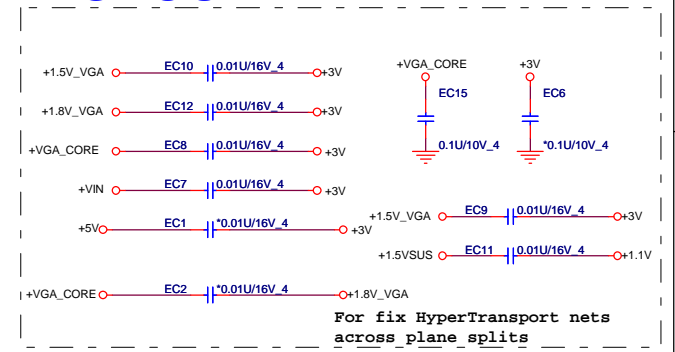
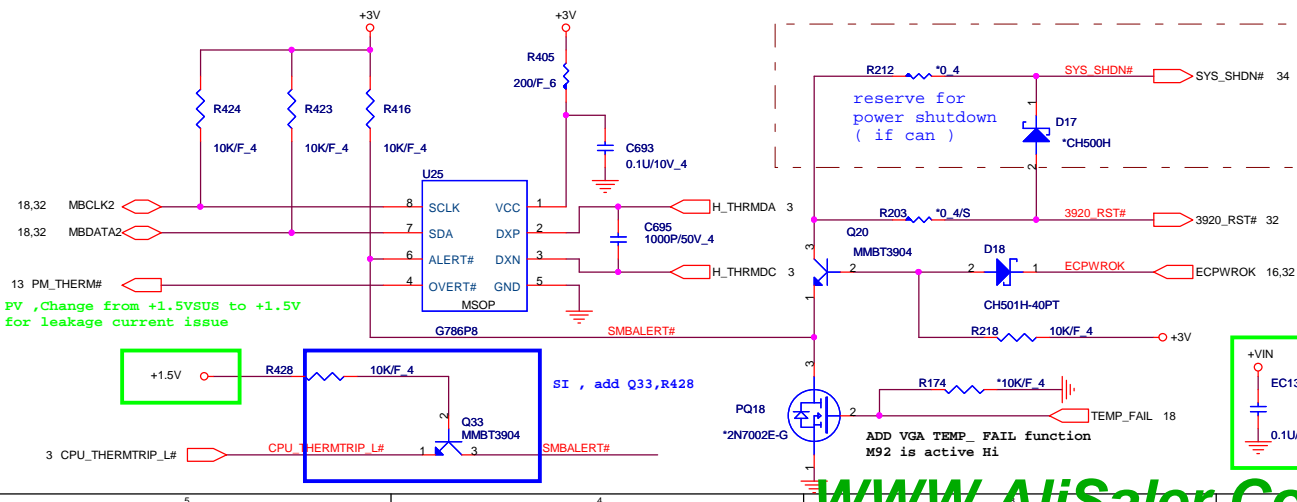
WWW.AliSaler.Com



Size Custom	Document Number <b>S1G4 DDRII MEMORY I/F 2/3</b>	Rev 1A
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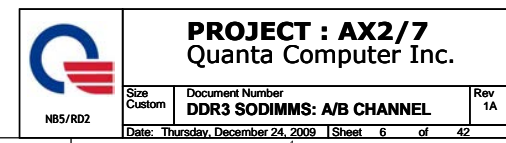
## PROCESSOR POWER AND GROUND



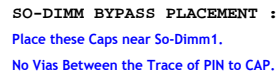
**PROJECT : AX2/7**  
Quanta Computer Inc.

Size Custom Document Number S1G4 PWR & GND 3/3 Rev 1A

Date: Thursday, December 24, 2009 Sheet 5 of 42

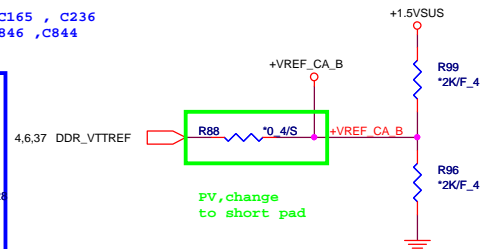





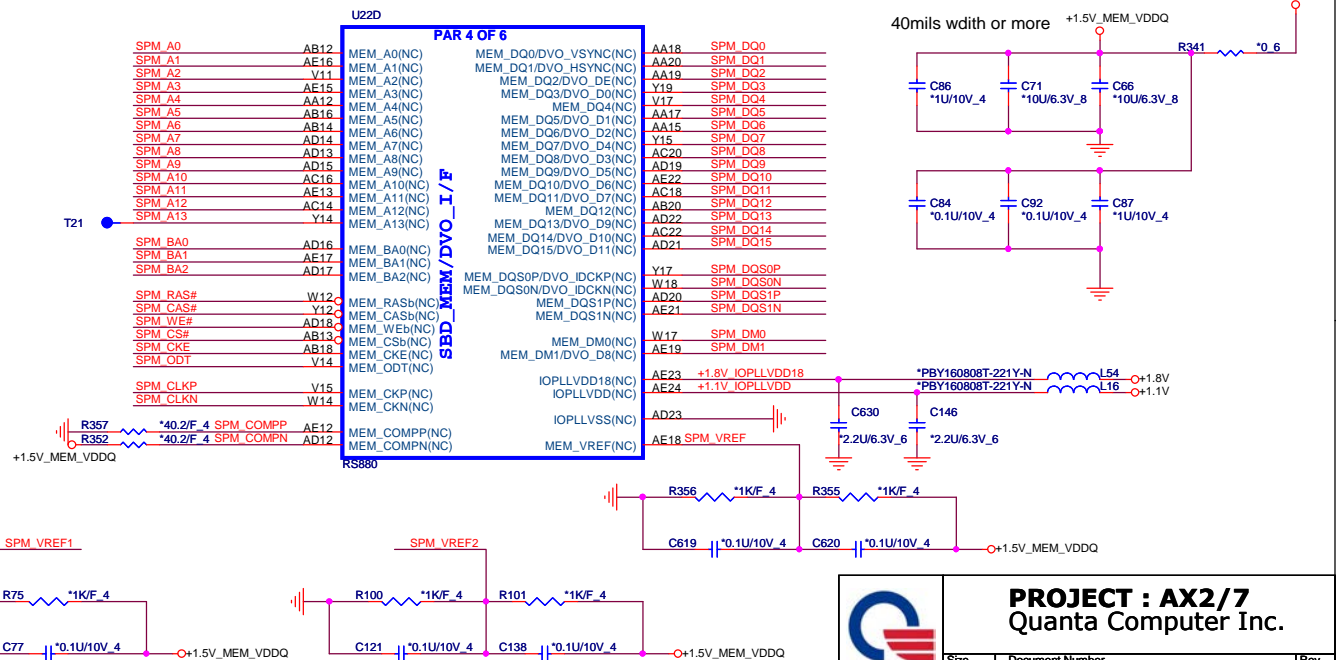
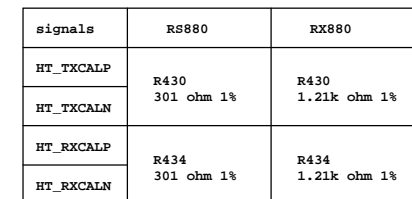


The diagram illustrates a decoupling network for DIMM2, consisting of a series of capacitors connected between a +1.5V supply and ground. The capacitors are labeled as follows:

- C197: .1U/10V\_4
- C151: .1U/10V\_4
- C127: .1U/10V\_4
- C198: .1U/10V\_4
- C152: .1U/10V\_4
- C128: .1U/10V\_4
- C229: .1U/10V\_4
- C166: .1U/10V\_4
- C140: .1U/10V\_4
- C225: .1U/10V\_4
- C167: .1U/10V\_4
- C141: .1U/10V\_4



 NBS/RD2	<b>PROJECT : AX2/7</b> Quanta Computer Inc.		
	Size Custom	Document Number <b>DDR3 SODIMMS TERMINATIONS</b>	Rev 1A
Date: Thursday, December 24, 2009   Sheet 7 of 42			





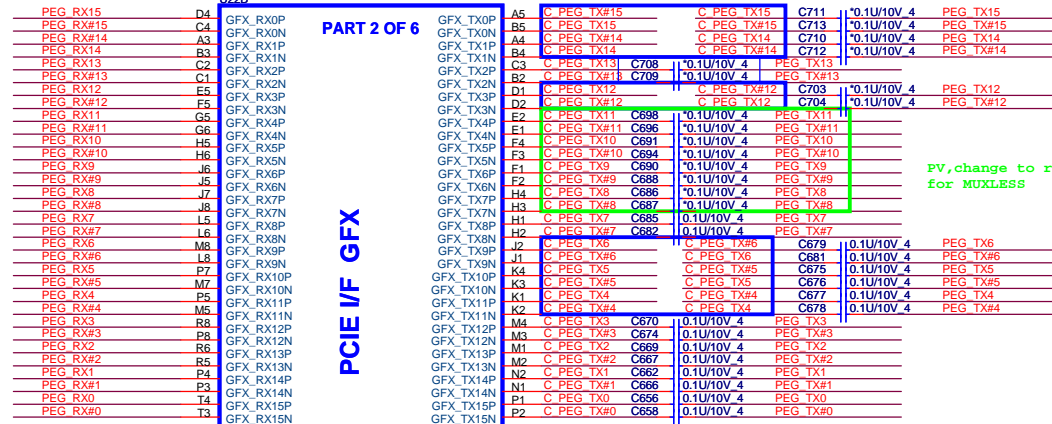
GFX\_RX can remove  
at next stage for MUXLESS

SI, for routing smooth  
GFX\_TX 0/1/3/9/10/11

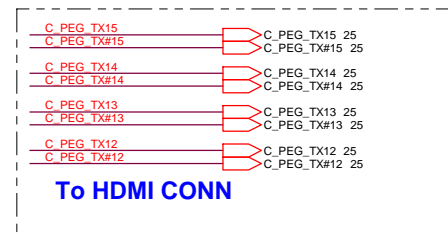
UMA can remove all GFX\_TX CAP  
SI remove C711,C713,C710,  
C712,C708,C709,C703,C704  
for MUXLESS

## PART 2 OF 6

## PCIe I/F GFX



Close to North Bridge



To HDMI CONN



TO WLAN  
TO PCIe-LAN

## PCIe I/F GPP

## PCIe I/F SB

PCE\_CALRP(PCE\_BCALRP)  
PCE\_CALRN(PCE\_BCALRN)

RS880

## RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1



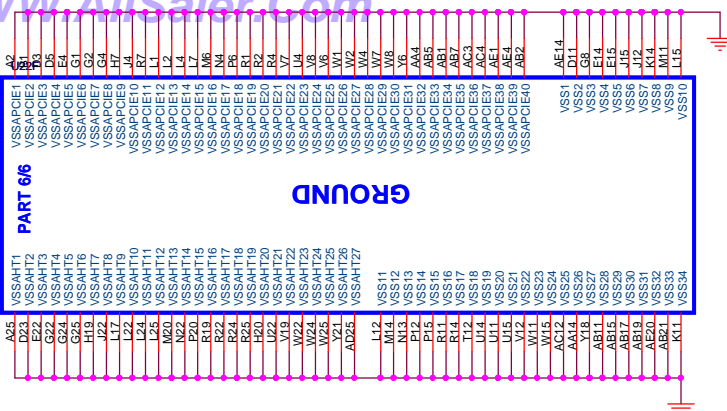
**PROJECT : AX2/7**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>RS880-PCIe I/F 2/5</b>	Rev 1A
Date: Thursday, December 24, 2009	Sheet 9 of 42	



RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLTP18	+1.8V
IOPLLVD18	+1.8V	VDDLTP33	NC



GROUND

VDDHT - HT  
LINK TX digital  
I/O for  
RX780/RS780

+1.1V 2A for RS880M

VDDHTRX - HT  
LINK RX I/O for  
RX780/RS780

0.7A

VDDHTTX - HT  
LINK TX I/O for  
RS880

+1.1V 2A for RS880M

+1.8V 1A for RS780M+SB700

VDDA18PCIE -  
PCIE TX stage  
I/O for  
RX780/RS780

VDD18 - RS780 I/O  
transform

VDD18\_MEM For UMA RS780 only  
Not applicable to RX780  
memory I/O transform

U22E

PART 5/6

POWER

RS880

VDDPCIE\_1

VDDPCIE\_2

VDDPCIE\_3

VDDPCIE\_4

VDDPCIE\_5

VDDPCIE\_6

VDDPCIE\_7

VDDPCIE\_8

VDDPCIE\_9

VDDPCIE\_10

VDDPCIE\_11

VDDPCIE\_12

VDDPCIE\_13

VDDPCIE\_14

VDDPCIE\_15

VDDPCIE\_16

VDDPCIE\_17

VDDC\_1

VDDC\_2

VDDC\_3

VDDC\_4

VDDC\_5

VDDC\_6

VDDC\_7

VDDC\_8

VDDC\_9

VDDC\_10

VDDC\_11

VDDC\_12

VDDC\_13

VDDC\_14

VDDC\_15

VDDC\_16

VDDC\_17

VDDC\_18

VDDC\_19

VDDC\_20

VDDC\_21

VDDC\_22

VDDC\_23

VDDC\_24

VDDC\_25

VDDC\_26

VDDC\_27

VDDC\_28

VDDC\_29

VDDC\_30

VDDC\_31

VDDC\_32

VDDC\_33

VDDC\_34

VDDC\_35

VDDC\_36

VDDC\_37

VDDC\_38

VDDC\_39

VDDC\_40

VDDC\_41

VDDC\_42

VDDC\_43

VDDC\_44

VDDC\_45

VDDPCIE - PCIE-E Main power

2.5A

VDDC - Core Logic power

7A

VDD\_MEM For UMA RS780 only  
Not applicable to RX780  
memory I/O transform

SI, change footprint to 0603

+1.5V VDD MEM

VDD\_MEM1(NC)

VDD\_MEM2(NC)

VDD\_MEM3(NC)

VDD\_MEM4(NC)

VDD\_MEM5(NC)

VDD\_MEM6(NC)

VDDG18\_1(VDD18\_1)

VDDG18\_2(VDD18\_2)

VDD18\_MEM1(NC)

VDD18\_MEM2(NC)

VDDG33\_1(NC)

VDDG33\_2(NC)

VDDG33\_3(NC)

VDDG33\_4(NC)

VDDG33\_5(NC)

VDDG33\_6(NC)

VDDG33\_7(NC)

VDDG33\_8(NC)

VDDG33\_9(NC)

VDDG33\_10(NC)

VDDG33\_11(NC)

VDDG33\_12(NC)

VDDG33\_13(NC)

VDDG33\_14(NC)

VDDG33\_15(NC)

VDDG33\_16(NC)

VDDG33\_17(NC)

VDDG33\_18(NC)

VDDG33\_19(NC)

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VDDG33\_146(NC)

VDDG33\_147(NC)

VDDG33\_148(NC)

VDDG33\_149(NC)

VDDG33\_150(NC)

VDDG33\_151(NC)

VDDG33\_152(NC)

VDDG33\_153(NC)

VDDG33\_154(NC)







SATA PORT 0,1,2,3  
can support AHCI  
mode

PLACE SATA AC COUPLING  
CAPS CLOSE TO SB820

SATA1

SATA ODD

PLVDD\_SATA--  
SATA PLL  
POWER

XTLVDD\_SATA-- SATA  
crystal power

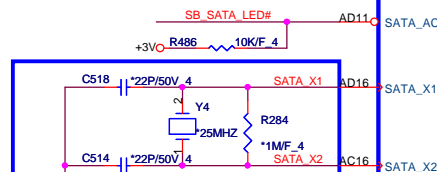


PLACE SATA CAL  
RES VERY CLOSE  
TO BALL OF SB820

NOTE:

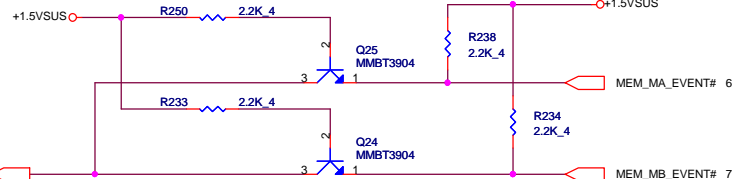
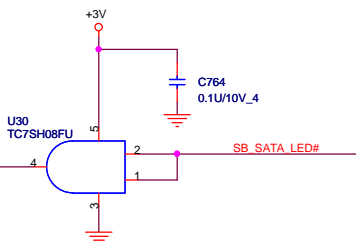
R361 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK

+1.1V\_AVDD\_SATA  
R476 1K/F 4  
R472 931/F 4  
SATA\_CALRP AB14  
SATA\_CALRN AA14



SI, change to reserve only

T72



SB800

Part 2 of 5

FLASH

SERIAL ATA

HW MONITOR

SPI ROM

IF THERE IS NO IDE, TEST  
POINTS FOR DEBUG BUS  
IS MANDATORY

SI define side port ID

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
1	0	0	Samsung
1	0	1	Hynix
0	0	0	No support side port

+3VS5 R259 \*10K/F 4 SIDE\_PORT\_ID0 R471 10K/F 4

+3VS5 R265 \*10K/F 4 SIDE\_PORT\_ID1 R475 10K/F 4

+3VS5 R264 \*10K/F 4 SIDE\_PORT\_ID2 R260 10K/F 4

+3VS5 R474 \*10K/F 4 BOARD\_ID0 R262 10K/F 4

R268 10K/F 4 BOARD\_ID1 R274 \*10K/F 4

R478 \*10K/F 4 BOARD\_ID2 R277 10K/F 4

R479 \*10K/F 4 BOARD\_ID3 R280 10K/F 4

R267 \*10K/F 4 BOARD\_ID4 R273 10K/F 4

For blue tooth  
& wireless  
merge card

SI define board ID

ID4	ID3	ID2	ID1	ID0	
0	0	0	0	0	AX2 UMA DF
0	0	0	0	1	AX7 UMA DF
0	0	0	1	0	AX2 PARK DF
0	0	0	1	1	AX7 PARK DF
0	0	1	0	0	AX2 UMA FF
0	0	1	0	1	AX7 UMA FF
0	0	1	1	0	AX2 PARK FF
0	0	1	1	1	AX7 PARK FF
0	1	0	1	0	AX2 M93 DF
0	1	0	1	1	AX7 M93 DF
0	1	1	1	0	AX2 M93 FF
0	1	1	1	1	AX7 M93 FF

FV define for M93



PROJECT : AX2/7  
Quanta Computer Inc.

Size  
Custom

Document Number  
SB820-ACPI/GPIO/USB 2/4

Rev  
1A

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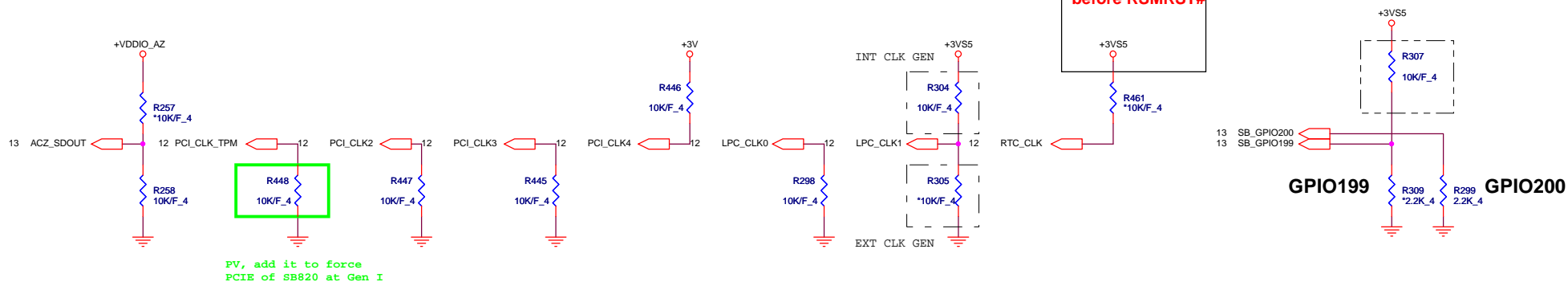




OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

internal have pull  
Hi 10K , confirm AMD  
ward this pull Hi  
not need

## REQUIRED STRAPS

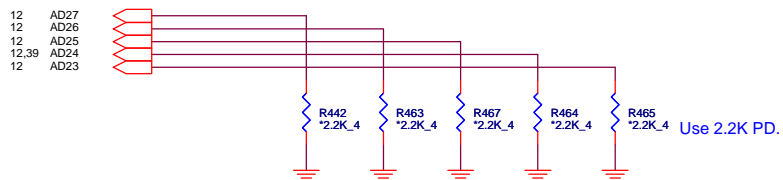


## REQUIRED STRAPS

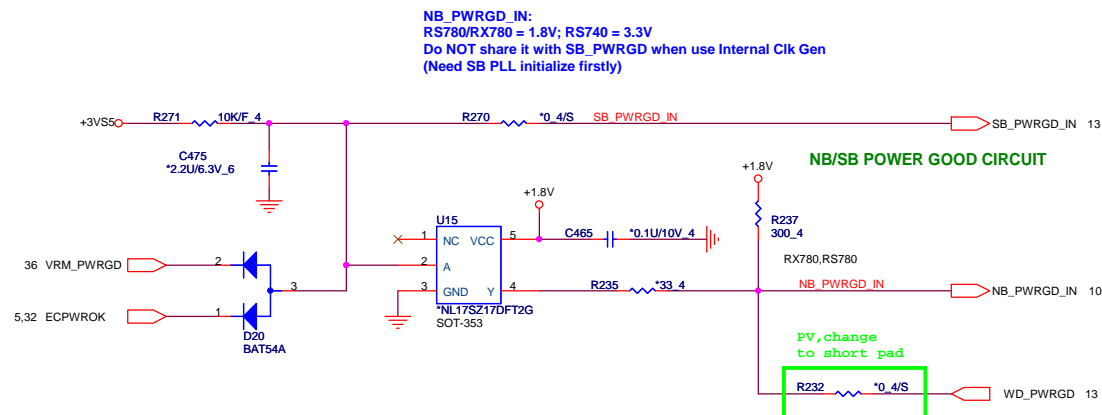
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

## DEBUG STRAPS

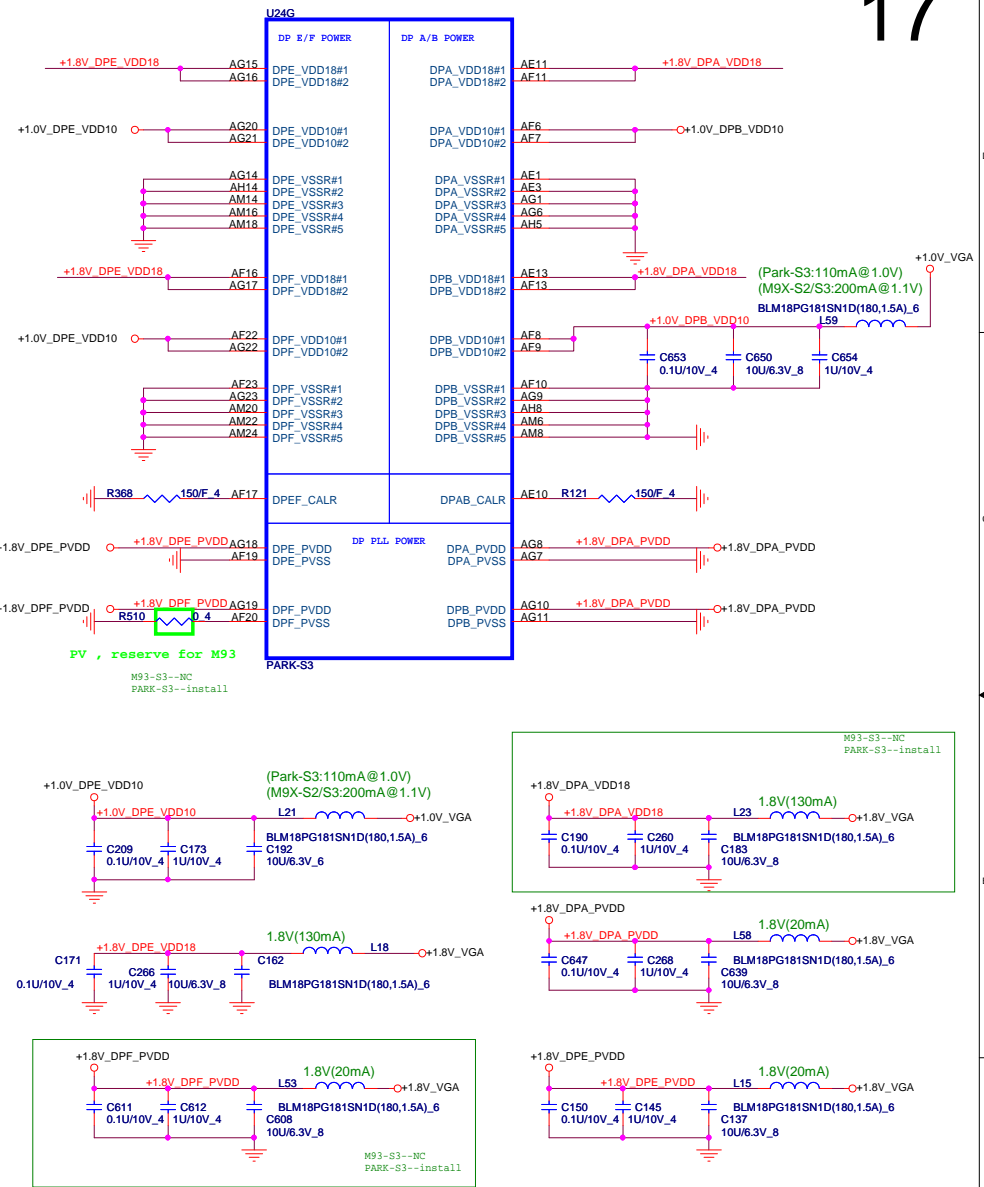
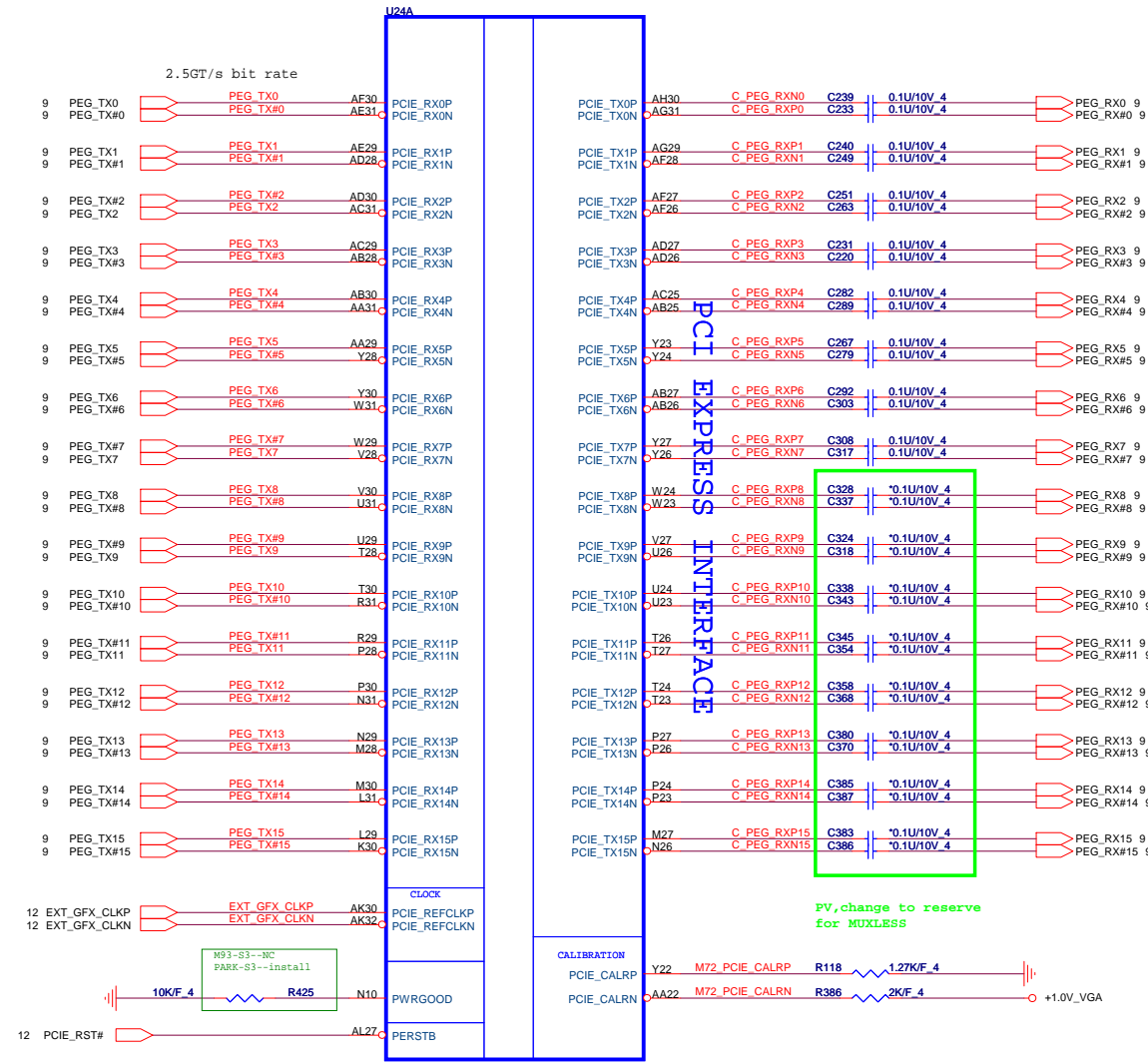
SB800 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

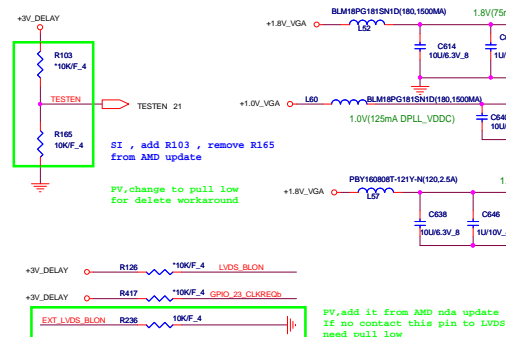
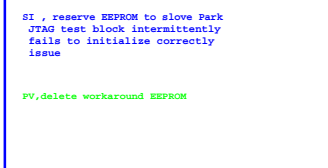
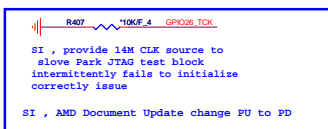
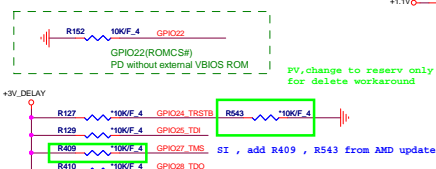


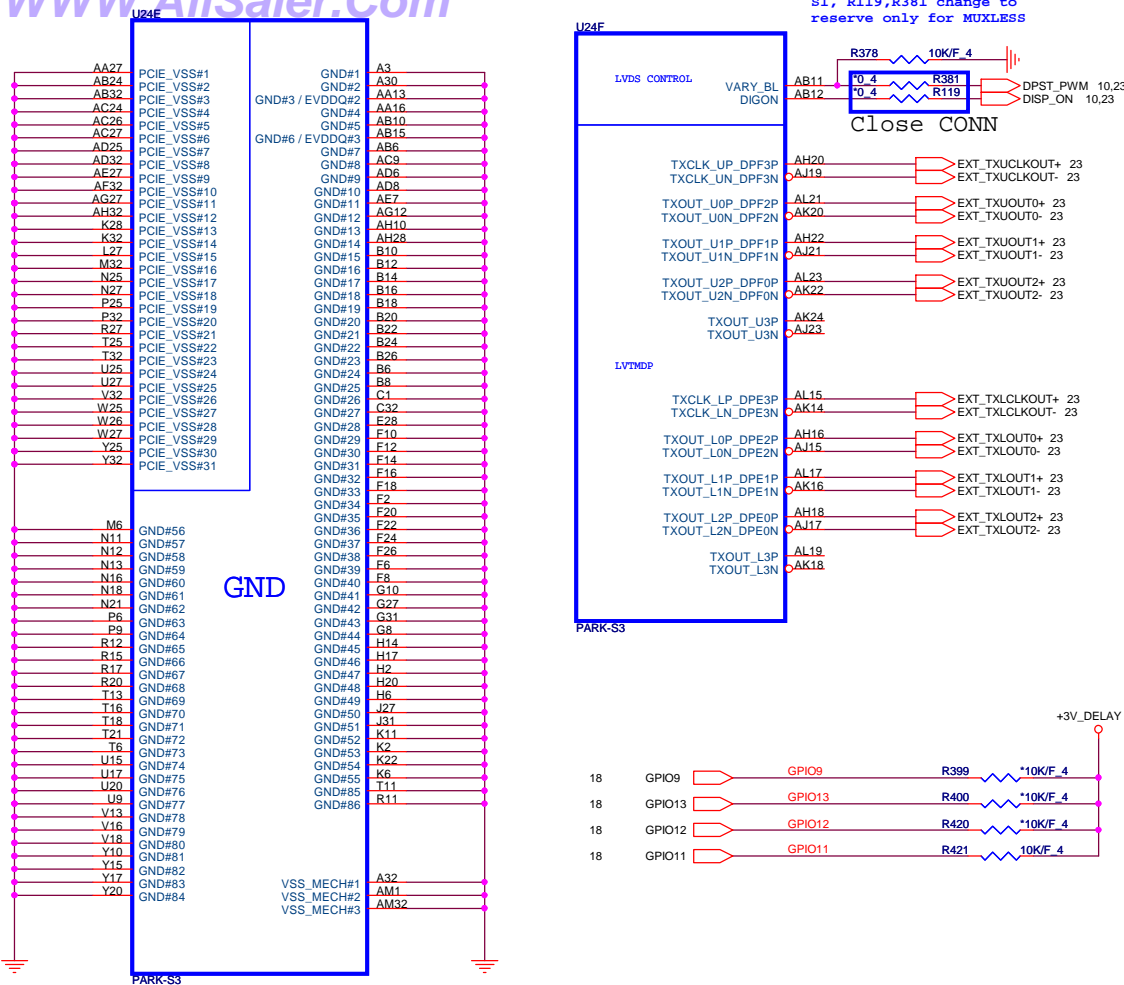
AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5



MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung- Bdie	8519=800MHz	R4W1C166D=NC11
0001	Hyundai- Orion	8516=800MHz	R770G65389R=1C
0010	Reserved		Reserved
0011	Reserved		Reserved
0100	Reserved		Reserved
0101	Reserved		Reserved
0110	Reserved		Reserved
0111	Reserved		Reserved
1000	Reserved		Reserved
1001	Reserved		Reserved
1010	Reserved		Reserved
1011	Reserved		Reserved
1100	Reserved		Reserved
1101	Reserved		Reserved
1110	Reserved		Reserved
1111	Reserved		Reserved

	PWRCTRL1	PWRCTRL0	V-CORE
L	0	0	0.9V
M	0	1	0.96V
H	1	0	1.06V
TBD	1	1	1.12V

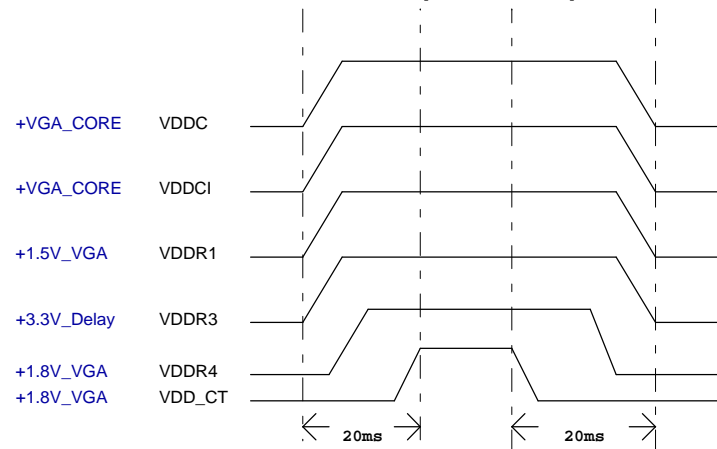




CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	<b>Transmitter Power Savings Enable</b> 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	<b>PCI Express Transmitter De-emphasis Enable</b> 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS		
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
H2SYNC	GENERICC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
GPIO21_BB_EN		

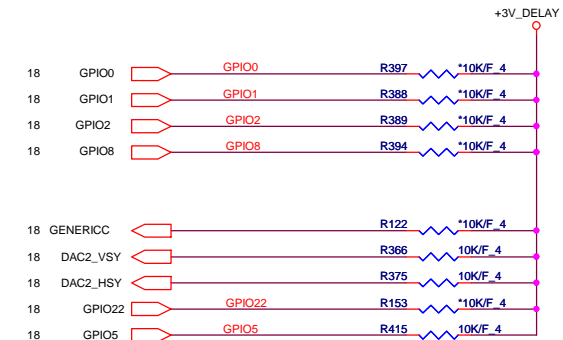
Power Up/Down Sequence



Memory Aperture size

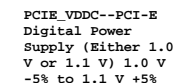
GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS\_ROM\_EN is set to 0.

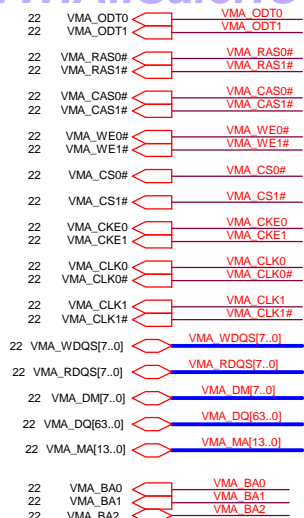


**PROJECT : AX2/7**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>PARK_GND / LVDS/ Straps</b>	Rev 1A
Date: Thursday, December 24, 2009	Sheet 19 of 42	

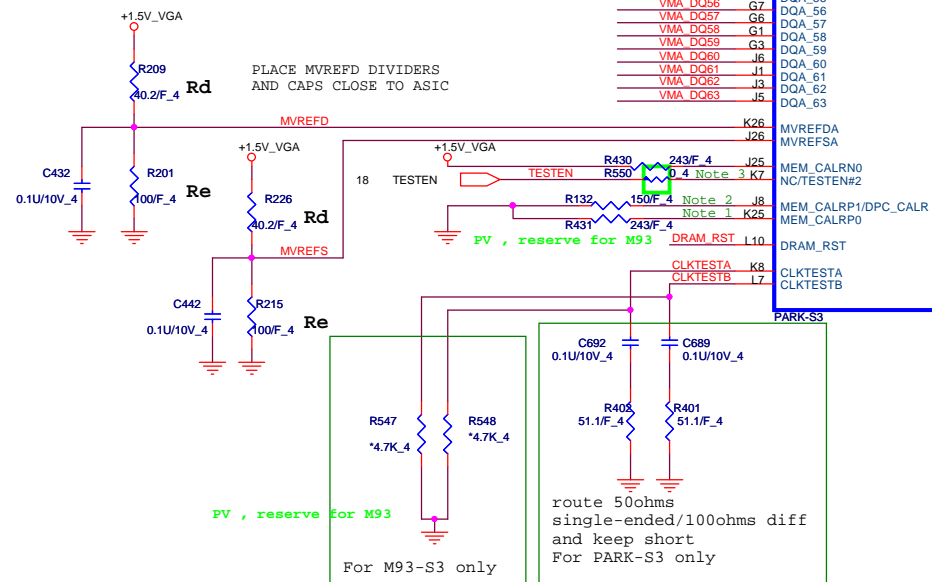




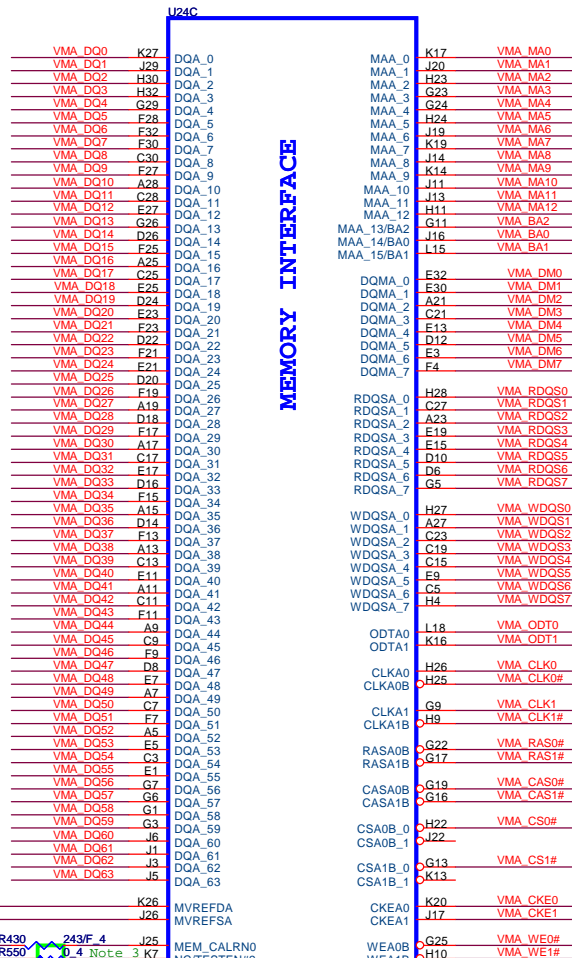


support 1gbt  
VRAM ( 64M X 16 )

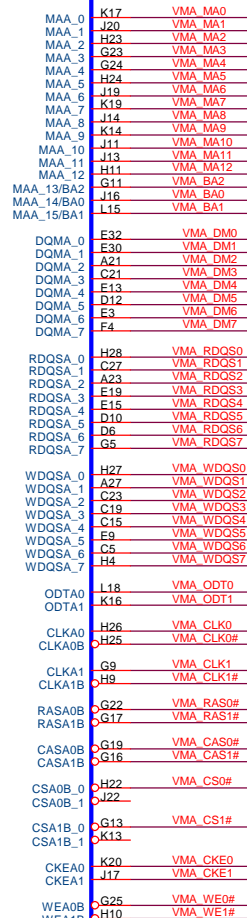
DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R



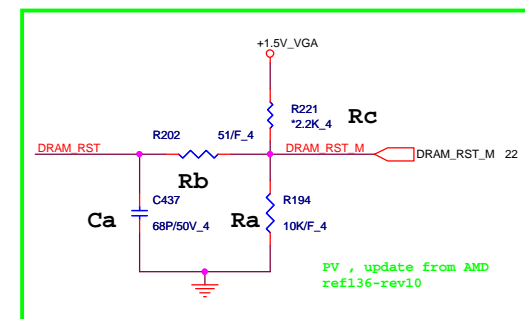
Note 1 :Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.  
Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.  
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC\_CALR  
Note 3 :For M9X-92/93, K7 Pin (NC\_MEM\_CALRP1) is Not connected.  
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST\_EN Signal At AF24



MEMORY INTERFACE



Designator	M9X-S2 and M93-S3	Park-S3
Ra	DNI	10K
Rb	0R/Short	51R
Rc	2.2K	DNI
Ca	2.2nF	68pF



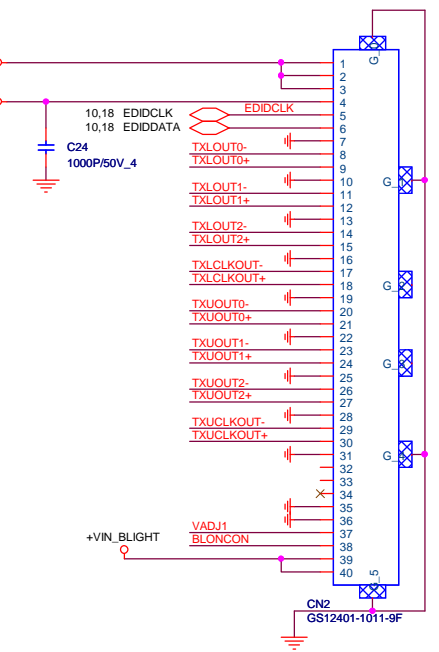
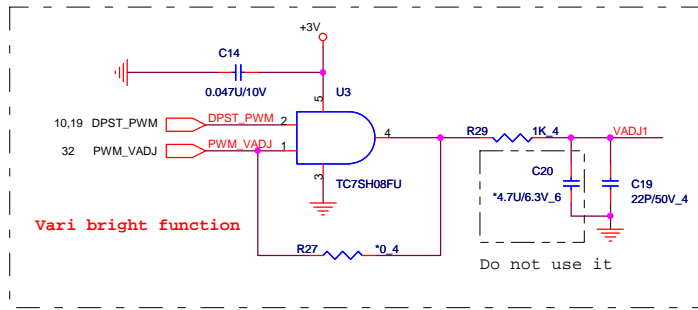
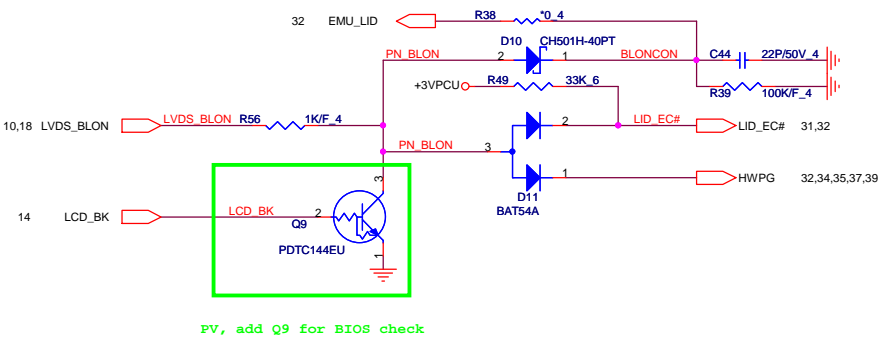
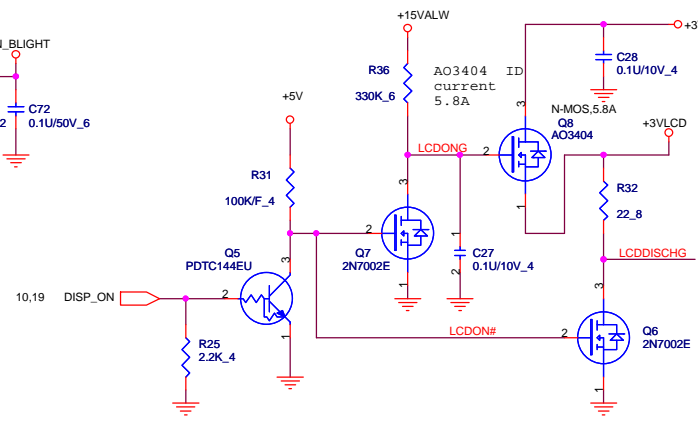
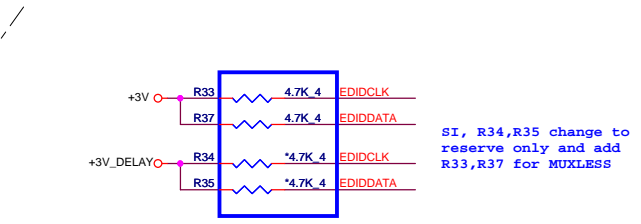
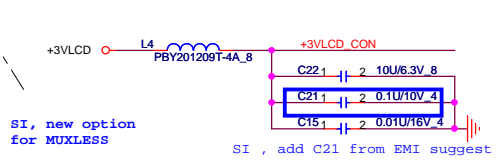
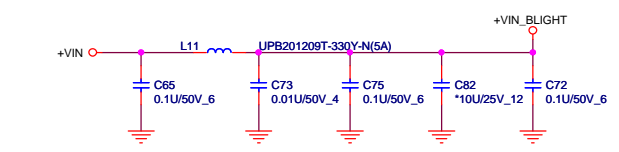
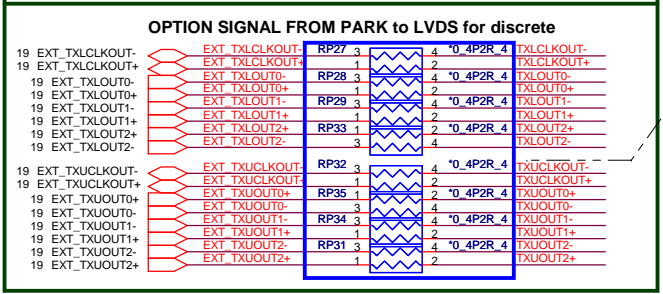
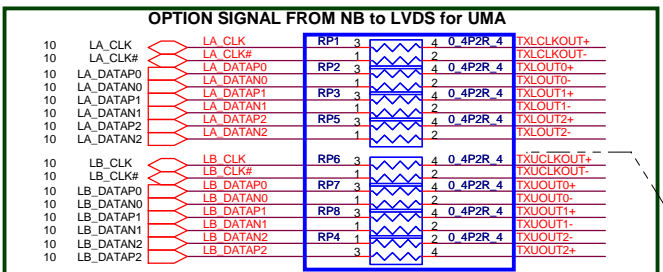
For PARK-S3 only  
For M9X-S2/S3 with  
DDR3: this pin is  
not in use.

**PROJECT : AX2/7**  
Quanta Computer Inc.

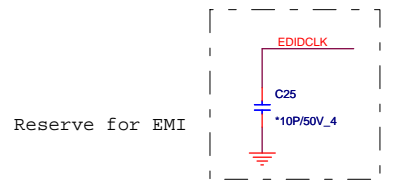
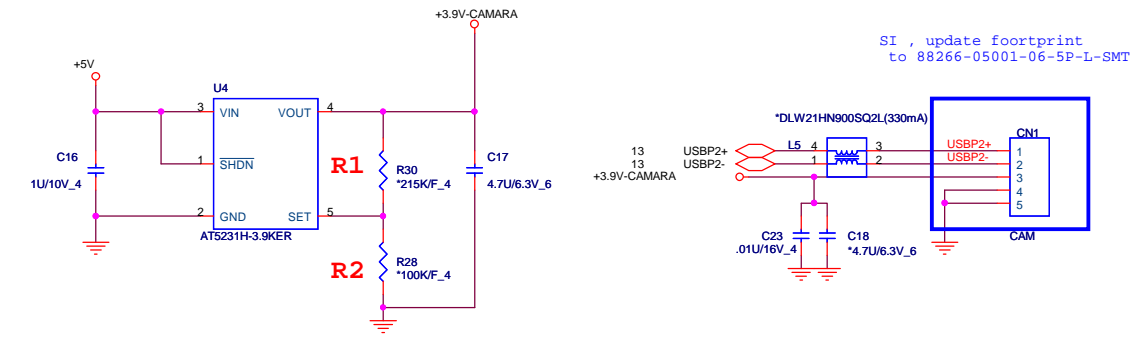
Size Custom	Document Number <b>PARK/MEM Interface</b>	Rev 1A
Date: Thursday, December 24, 2009 Sheet 21 of 42		



1. If LCD connector near GPU, then place these series Resistors near GPU  
2. If LCD connector near N/B, then place these series Resistors near N/B



# CAMERA



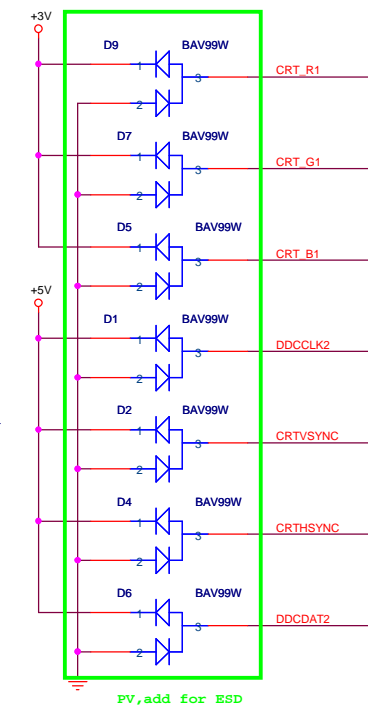
**PROJECT : AX2/7**  
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
LCD CONN		
Date: Thursday, December 24, 2009	Sheet 23	of 42

PV, change footprint  
to F3 2X1 65-2 8

PV , change footprint to  
dsub-dsd-15aebb-15p-v-smt

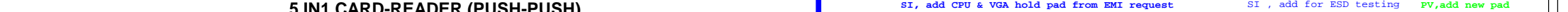
A microstrip layout for a fuse. A red line represents the microstrip, starting from a +5V pad on the left. It passes through via 2, then a gap, then via 1, and continues to the right. The gap between vias 1 and 2 is labeled "40 mils" in red. A blue zigzag line labeled "F1" is placed over the gap. Below the gap, the text "FUSE1A6V\_POLY" is written in blue.



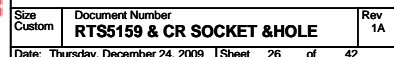
SI, R4,R10 change  
to reserve only and  
add R3,R9 for MUXLESS

SI, remove R93 , R350 . Add RP30  
R94,R351,Q14,Q15 change to  
reserve only for MUXLESS

PV,change to short pad



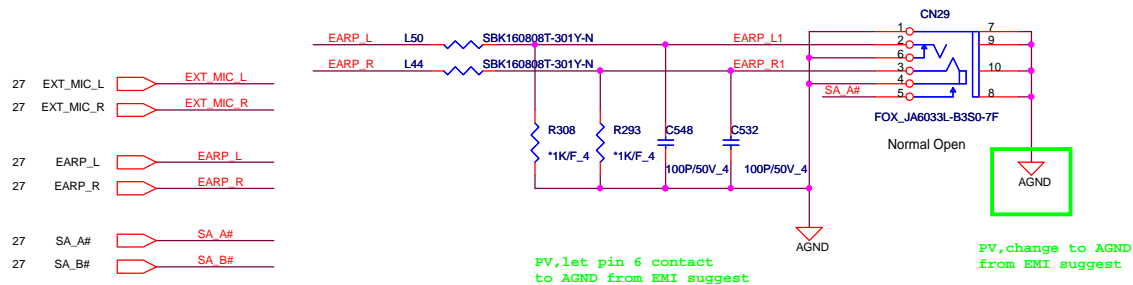
PV,add new pad  
for new outline







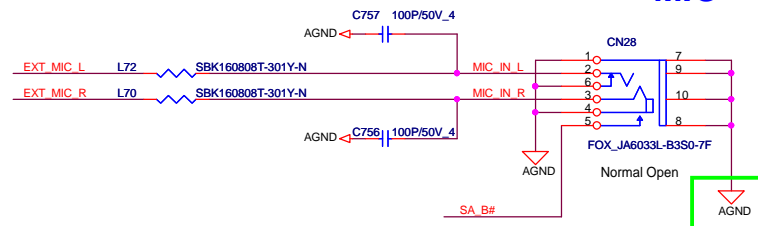
## Line out



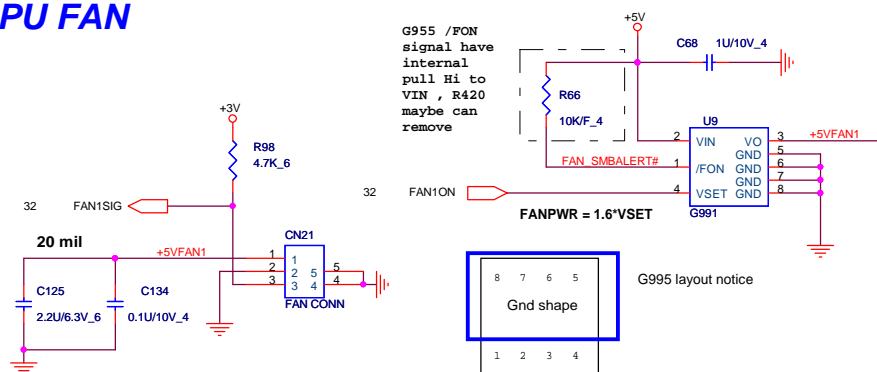
## MIC

SA\_A# --&gt; EXT Ear Phone

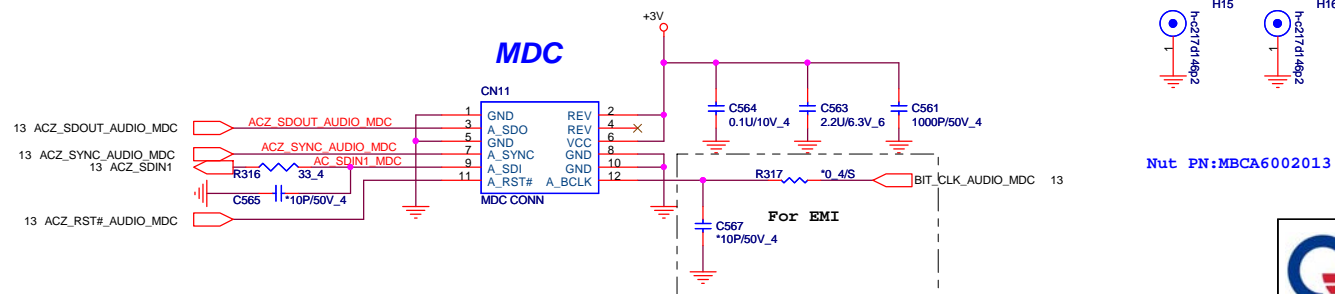
SA\_B# --&gt; EXT MIC



## CPU FAN

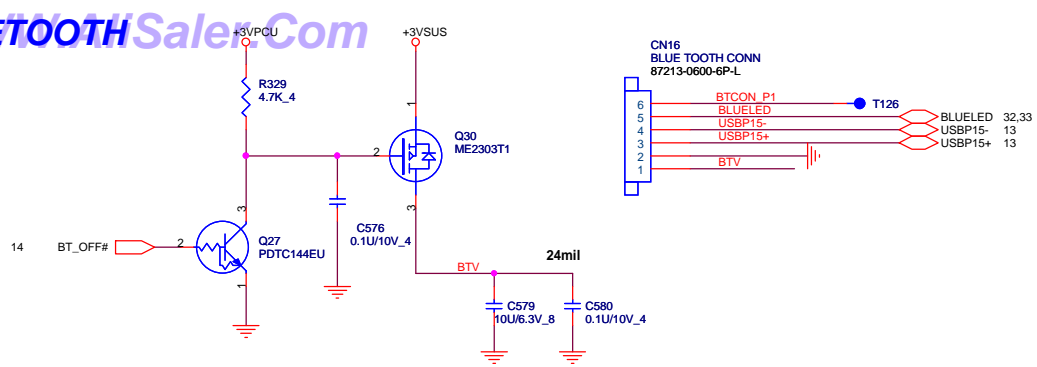


## Modem CONN

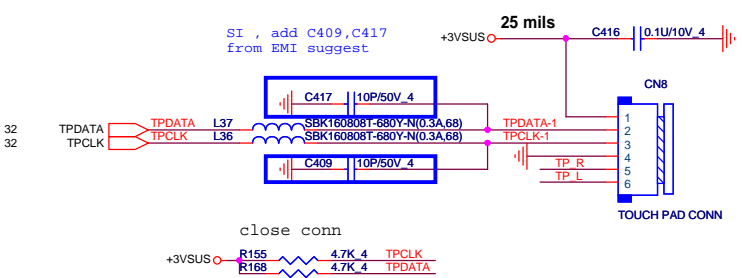


**PROJECT : AX2/7**  
Quanta Computer Inc.

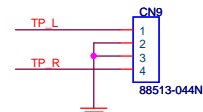
Size	Document Number	Rev
Custom	AMP_TPA6017/MDC1.5/CPU FAN	1A
Date: Thursday, December 24, 2009	Sheet 28 of 42	



## TOUCH PAD CONN



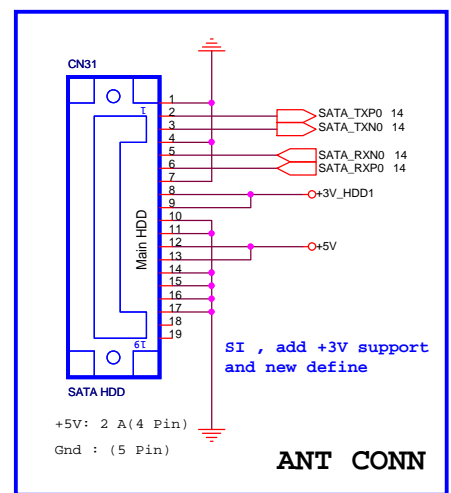
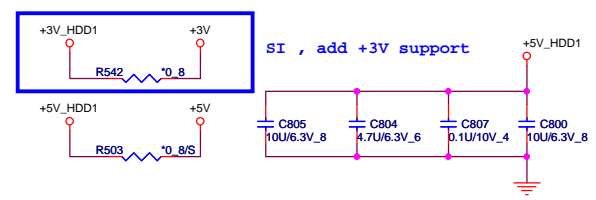
## To TOUCH PAD SW board



## SATA HDD CONNECTOR

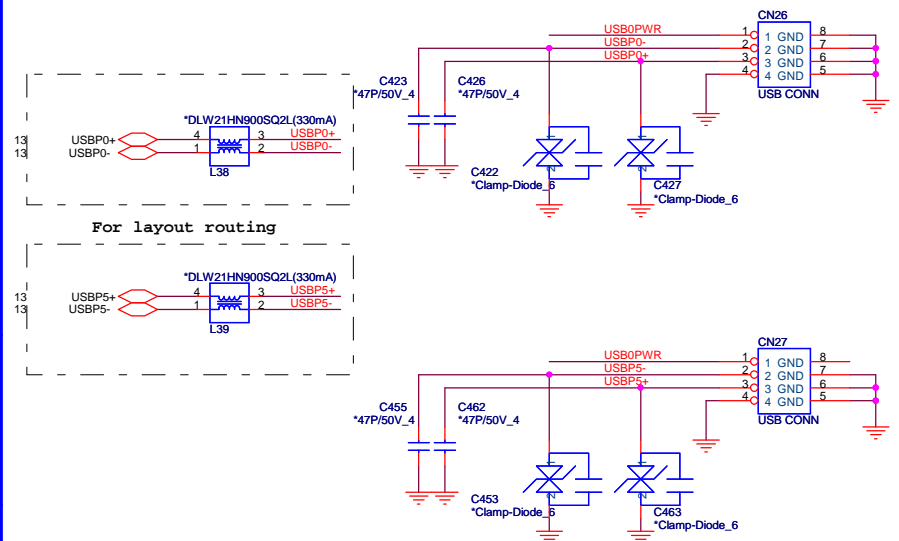
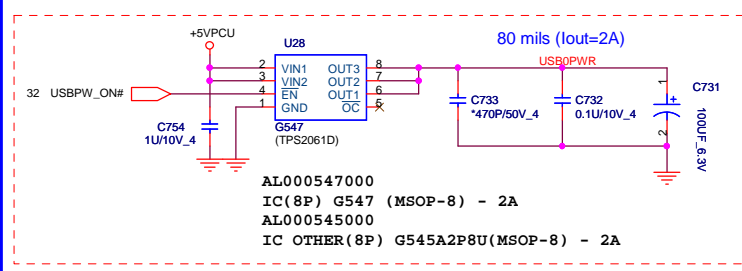
SI, update P/N : DFHS13FS019

SI, delete CN30 change to ANT CONN

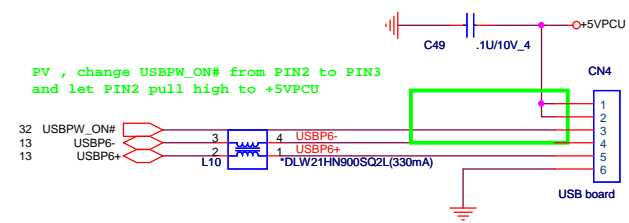



## ANT CONN

## LEFT SIDE USBX2



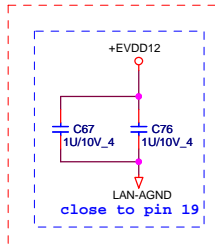
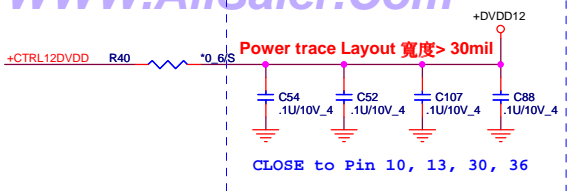
## Right SIDE USBX1



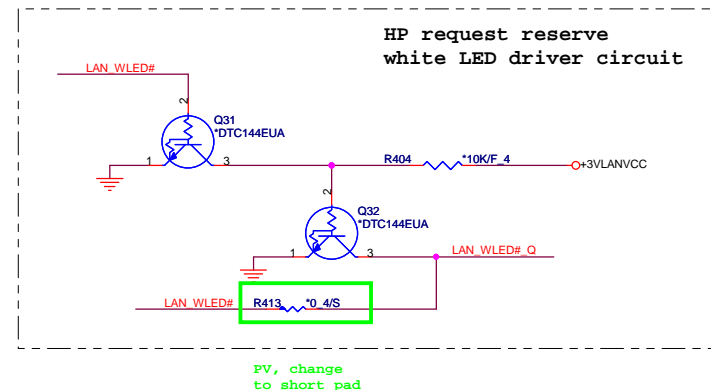
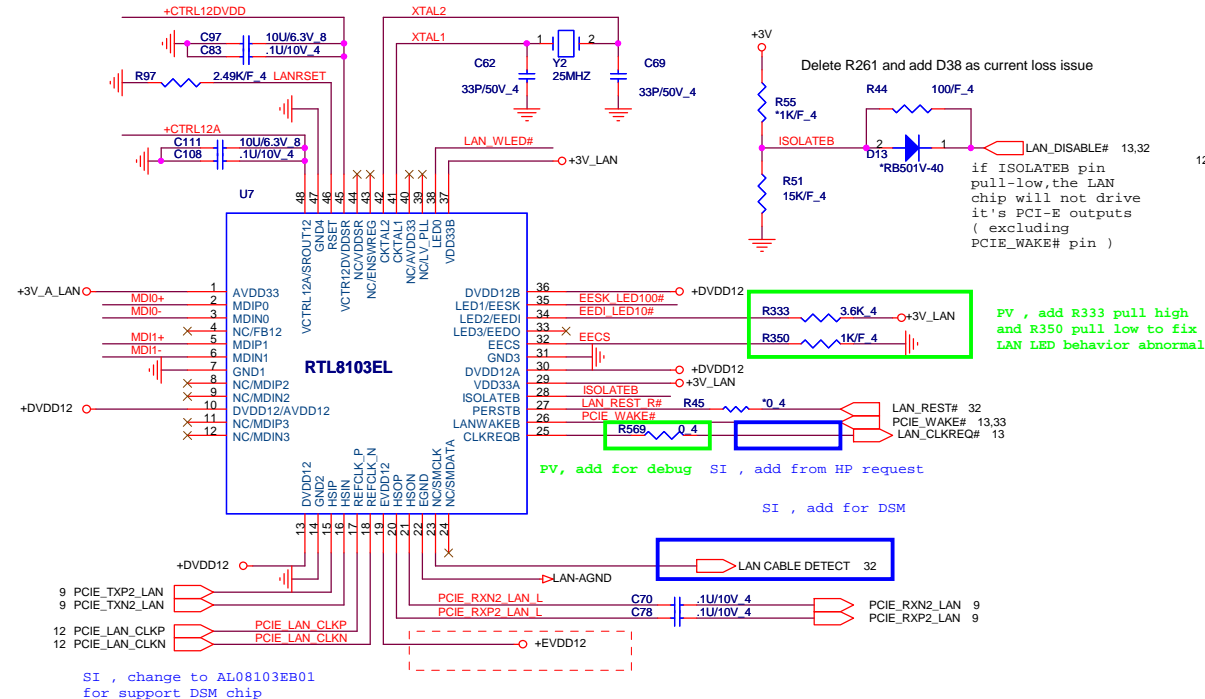
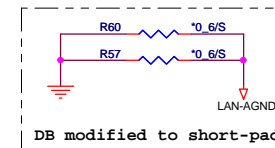
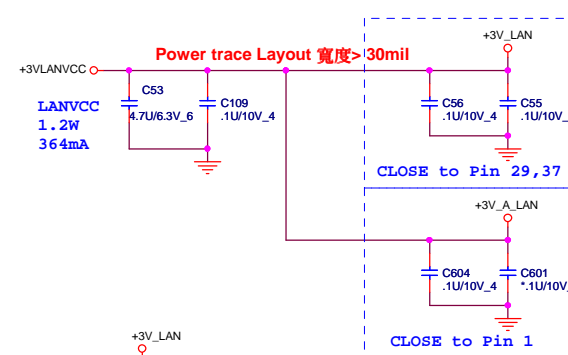


**PROJECT : AX2/7**  
Quanta Computer Inc.

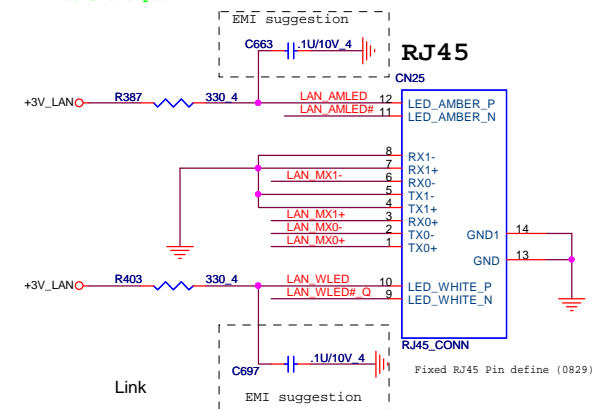
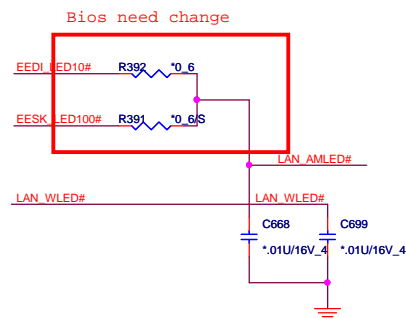
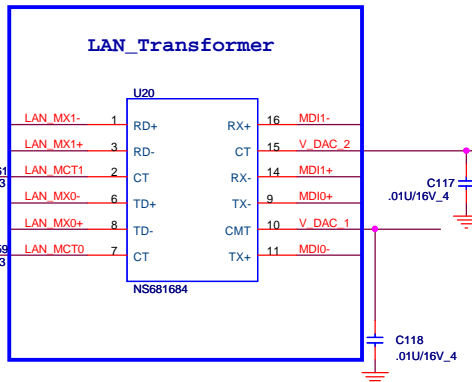
Size Custom	Document Number <b>BT/USBX3/TP/HDD</b>	Rev 1A
Date: Thursday, December 24, 2009   Sheet 29 of 42		



SI , remove EEPROM  
U5,C48,R42,R50

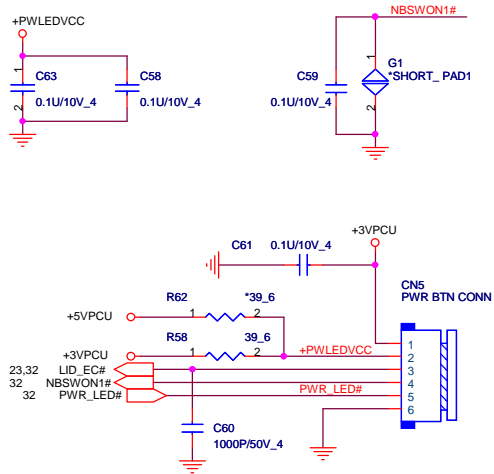


Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
LED0	O	57	38	LED0 Tx/Rx
LED1	O	56	35	LED1 Tx/Rx
LED2	O	55	34	LED2 Tx/Rx
LED3	O	54	33	LED3 Tx/Rx



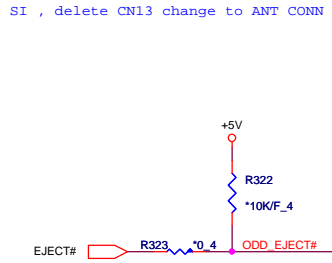
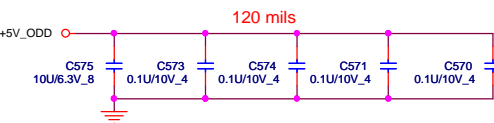
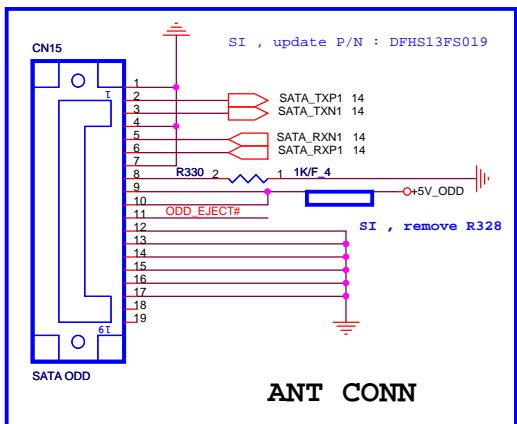
**PROJECT : AX2/7**  
Quanta Computer Inc.

Size Custom	Document Number RTL8102EL/RJ45	Rev 1A
Date: Thursday, December 24, 2009 Sheet 30 of 42		

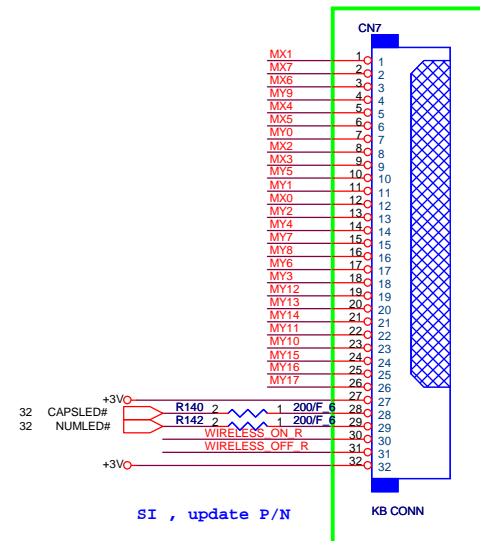
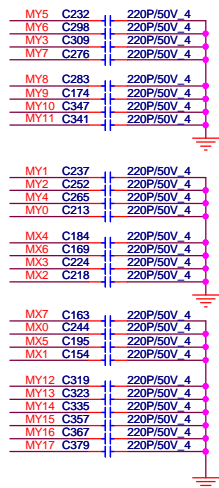


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

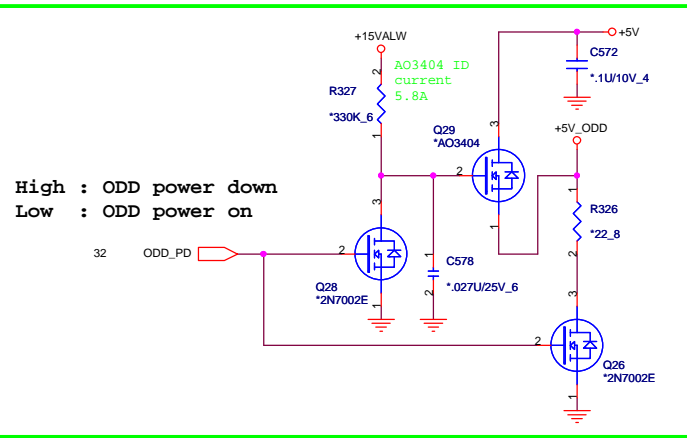
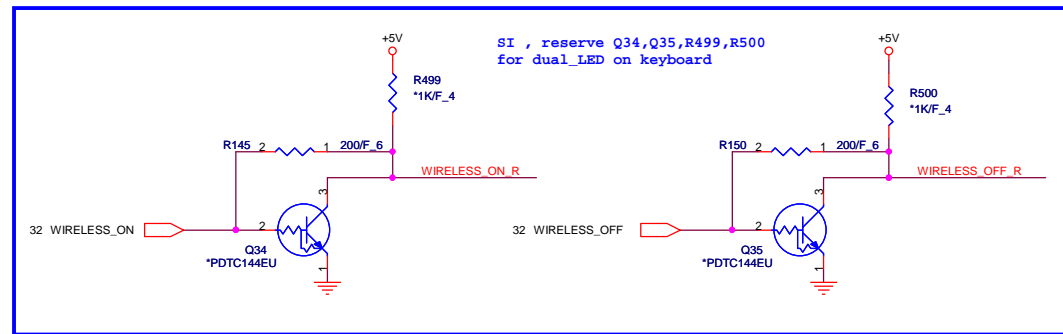
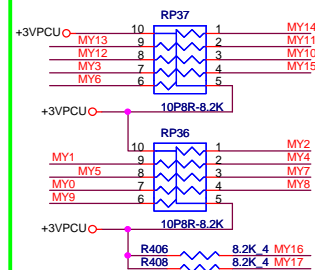
## SATA CD-ROM



## KEYBOARD CONN



## KEYBOARD PULL-UP



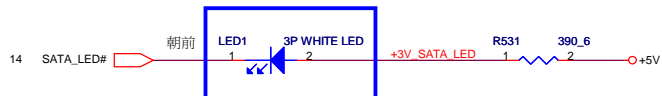
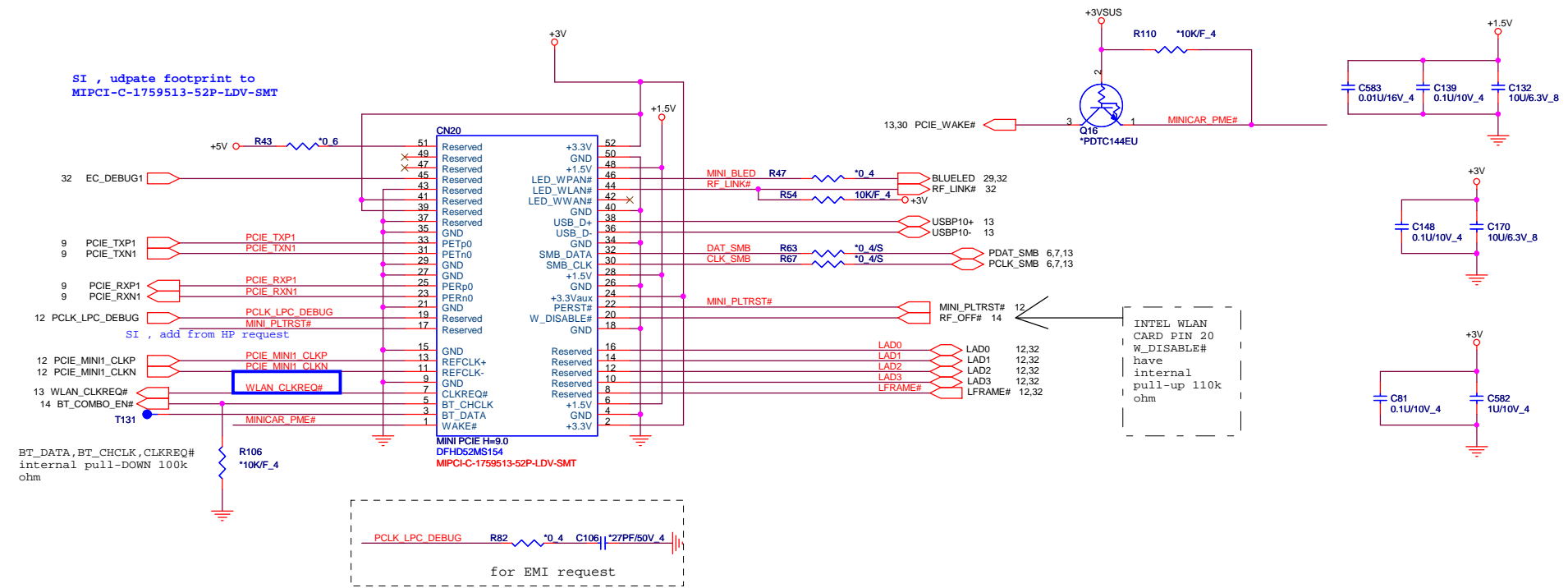
PV, change to reserve only

**PROJECT : AX2/7**  
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
KEYBOARD/SW_BOARD/ODD		
Date: Thursday, December 24, 2009 Sheet 31 of 42		



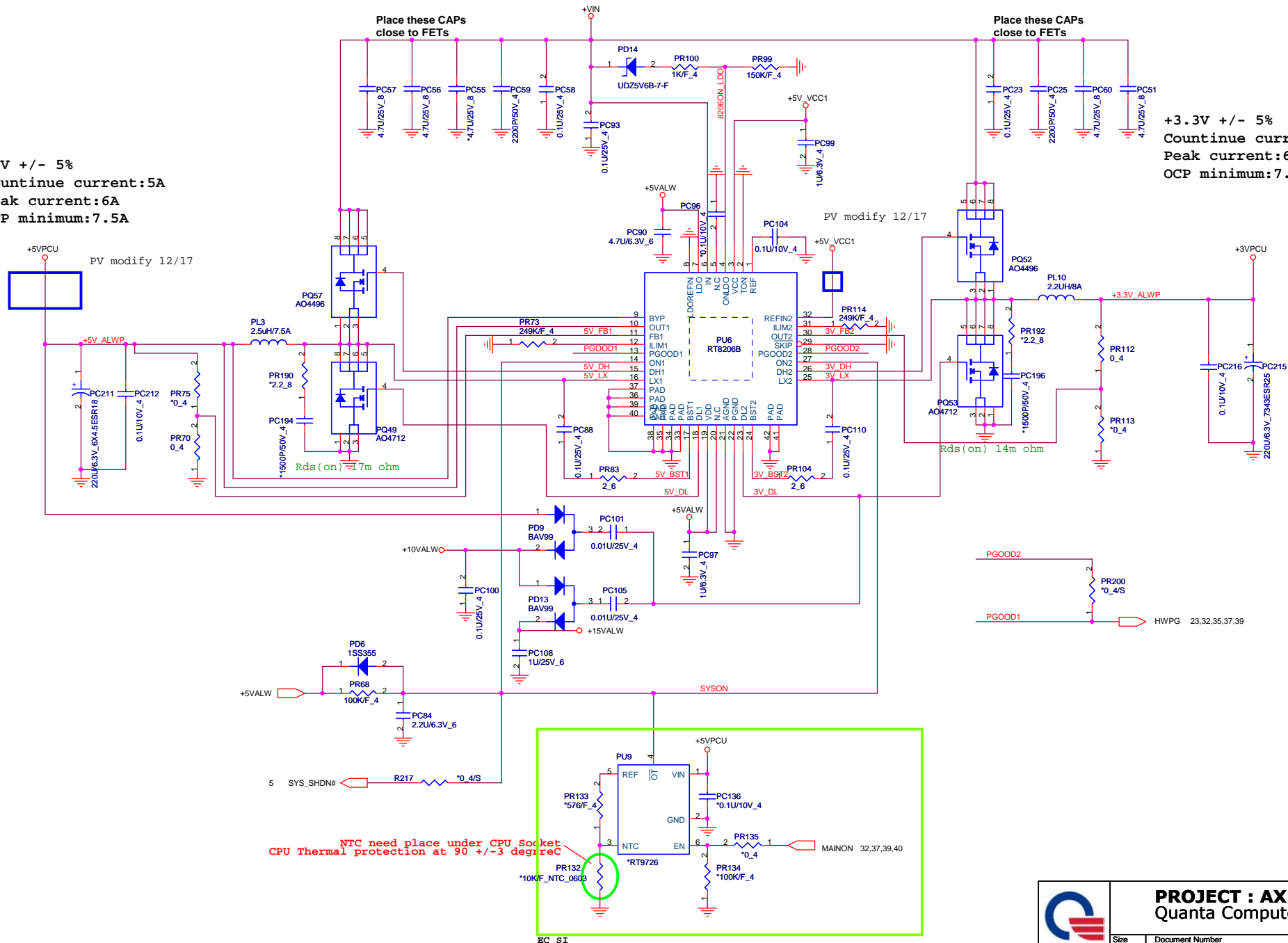




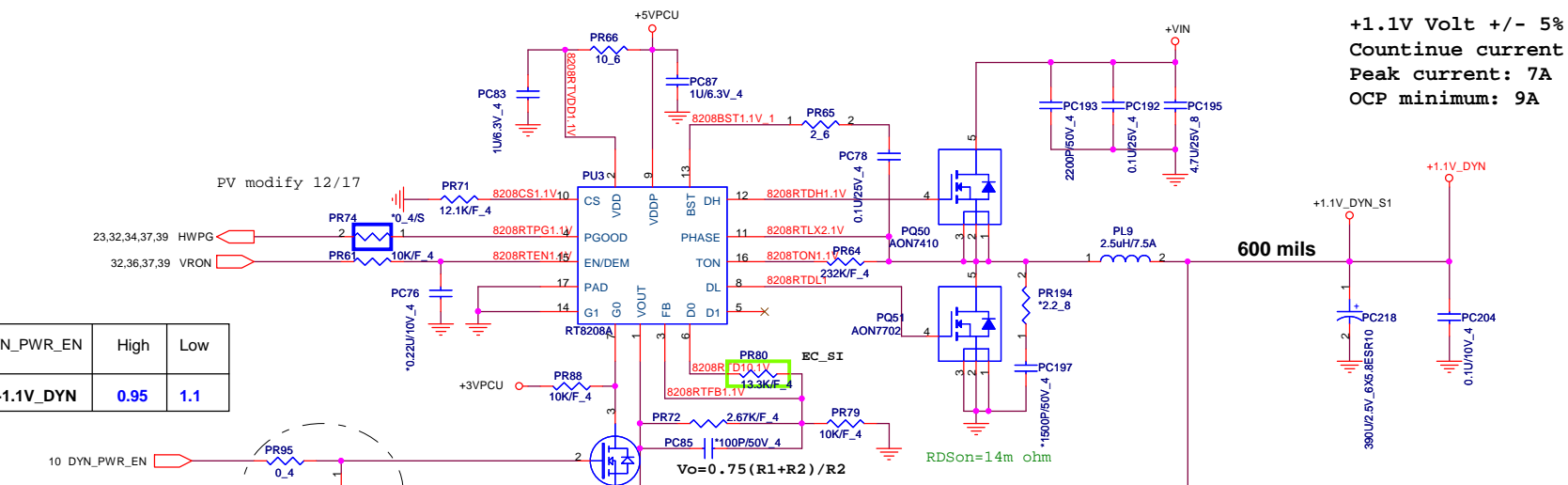
SI , change footprint to led1-s110kgct-3p-nb5

+5V +/- 5%  
Countinue current:5A  
Peak current:6A  
OCP minimum:7.5A

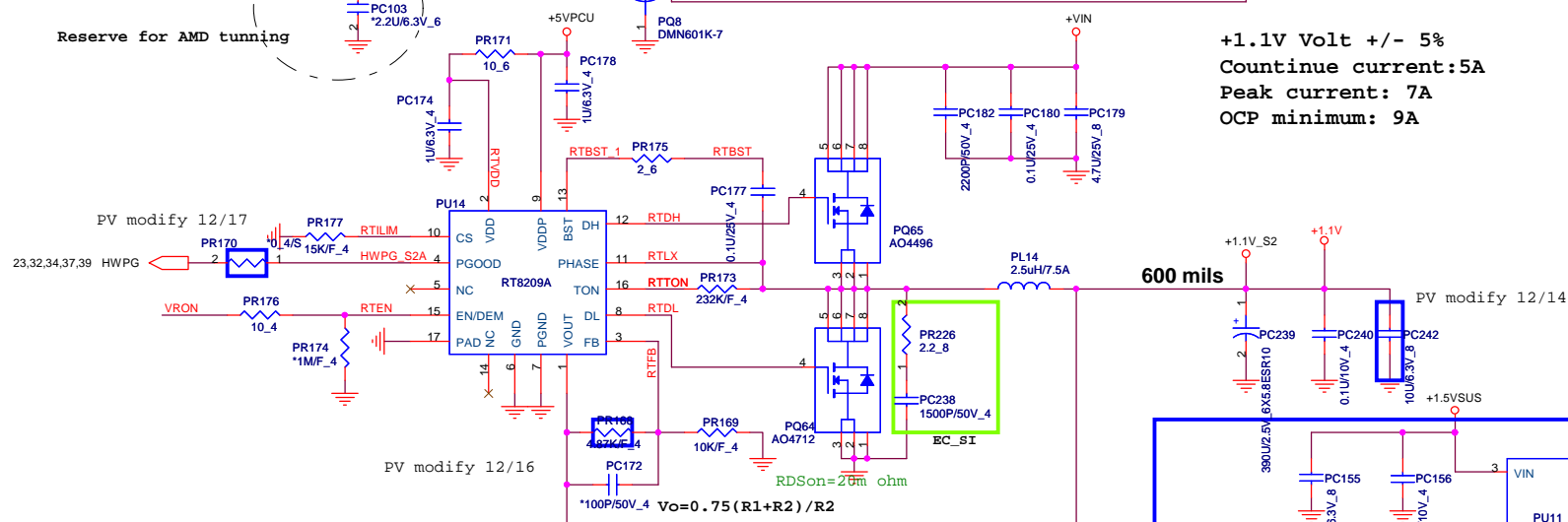
+3.3V +/- 5%  
Countinue current:5A  
Peak current:6A  
OCP minimum:7.5A



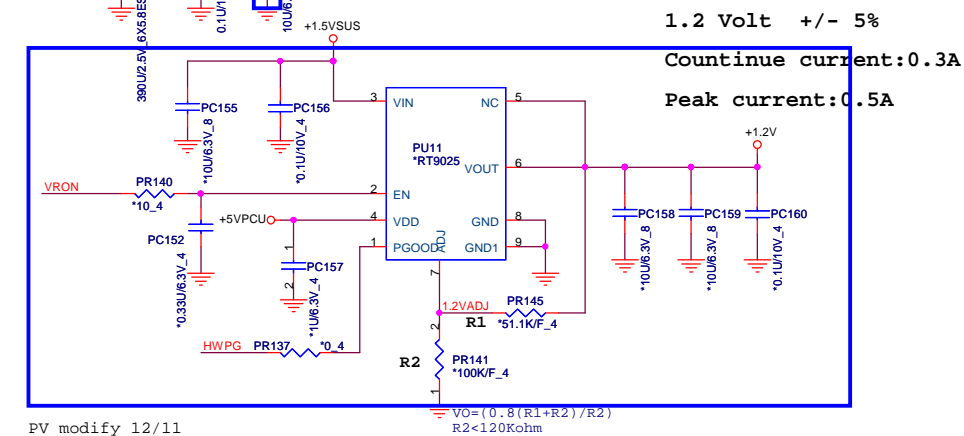
DYN_PWR_EN	High	Low
<b>+1.1V_DYN</b>	<b>0.95</b>	<b>1.1</b>



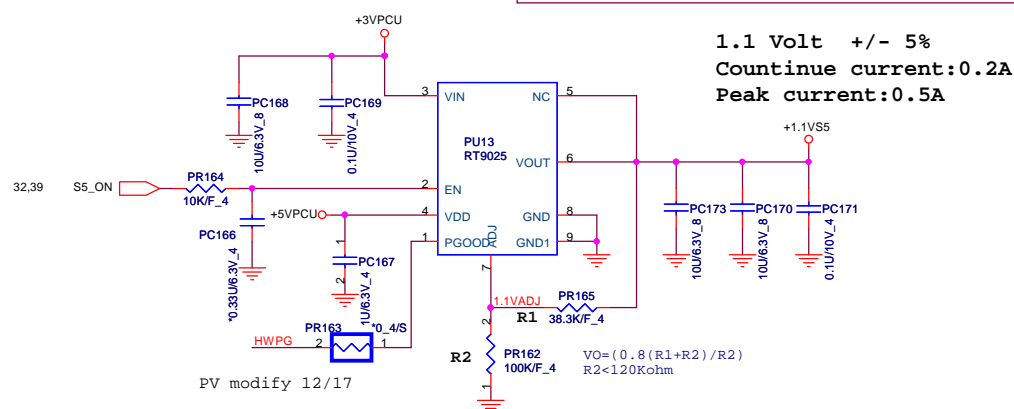
+1.1V Volt +/- 5%  
Continue current: 5A  
Peak current: 7A  
OCP minimum: 9A



+1.1V Volt +/- 5%  
Continue current: 5A  
Peak current: 7A  
OCP minimum: 9A

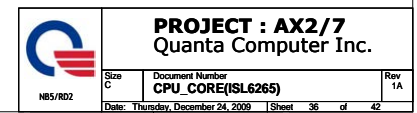


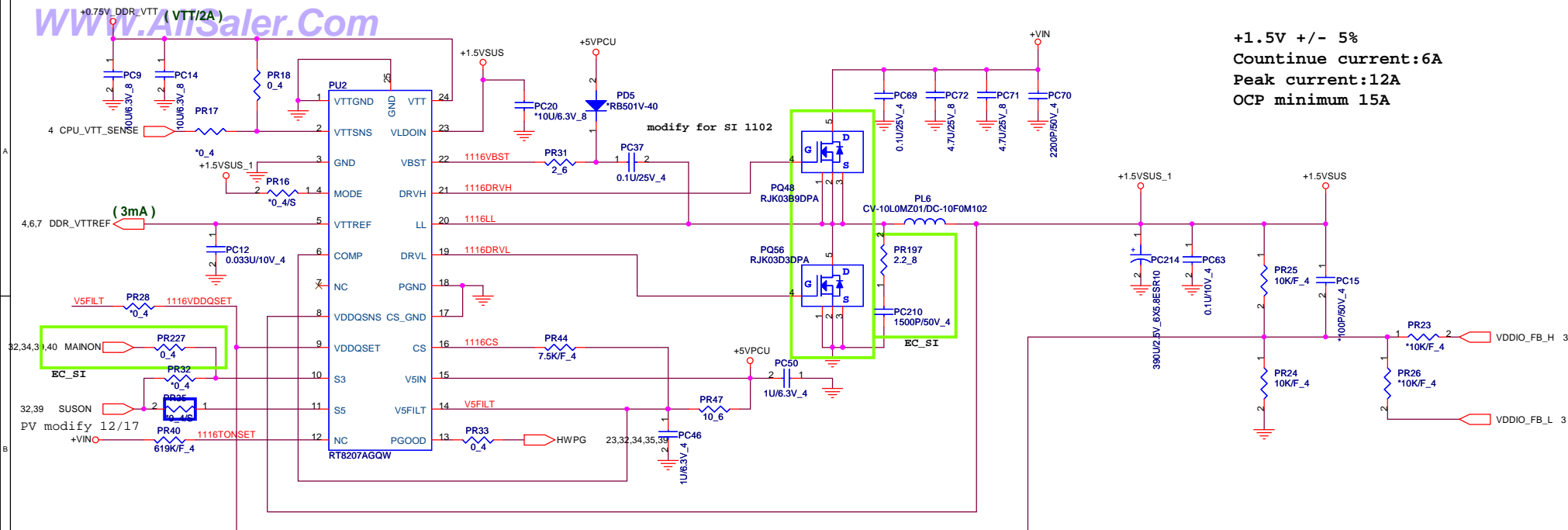
1.2 Volt +/- 5%  
Continue current: 0.3A  
Peak current: 0.5A



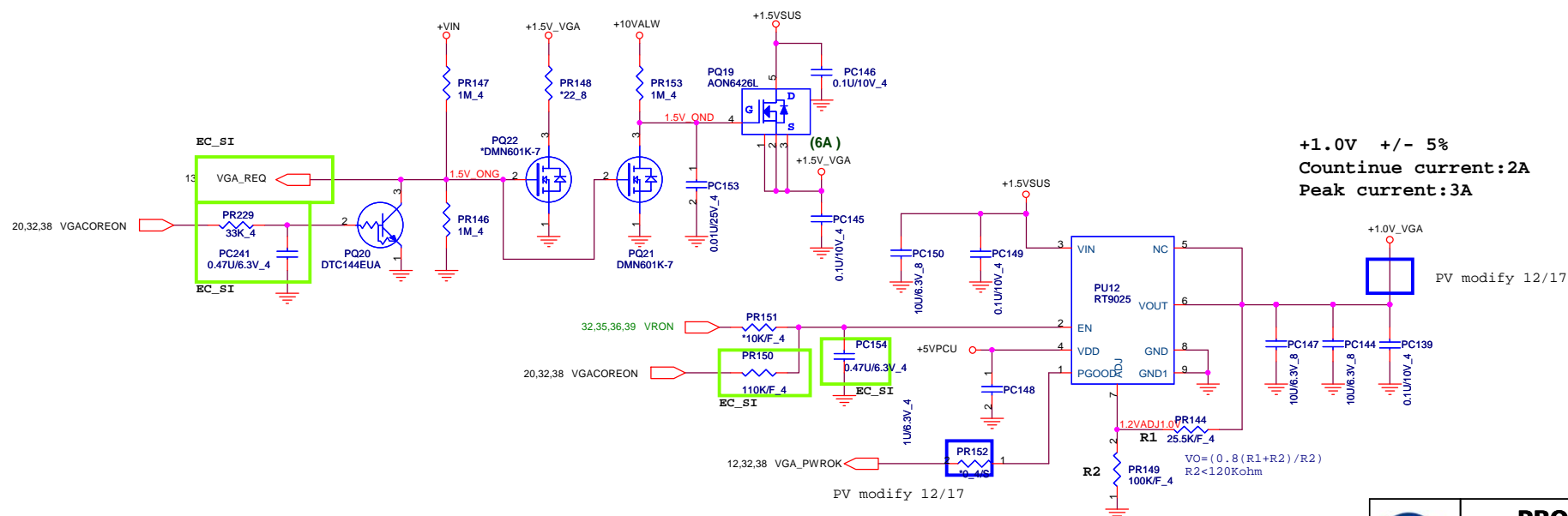
1.1 Volt +/- 5%  
Continue current:0.2A  
Peak current:0.5A

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8





+1.5V +/- 5%  
Continue current:6A  
Peak current:12A  
OCP minimum 15A



+1.0V +/- 5%  
Continue current:2A  
Peak current:3A

PV modify 12/17



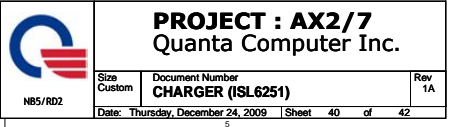
**PROJECT : AX2/7**  
Quanta Computer Inc.  
**SANTOS INTEL**

Size	Document Number <b>DDR3 (RT8207)</b>	Rev 1A
Date: Thursday, December 24, 2009	Sheet 37	of 42

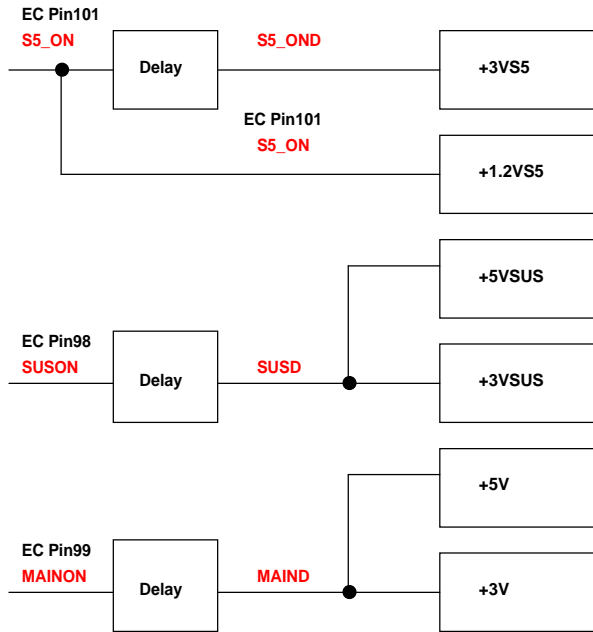
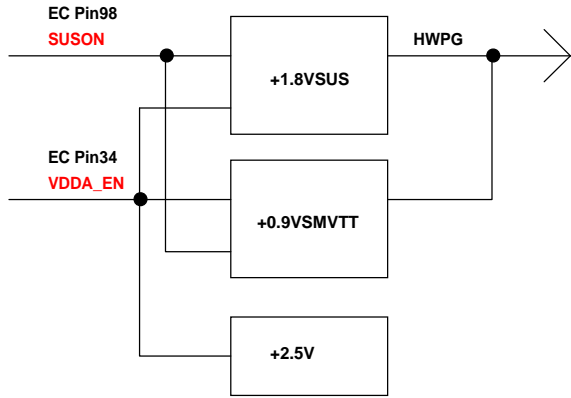




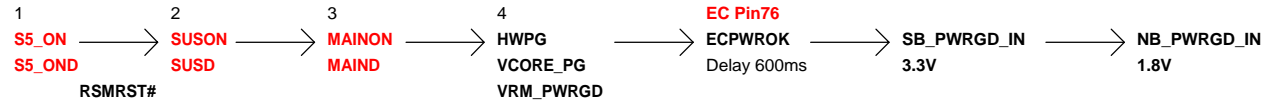
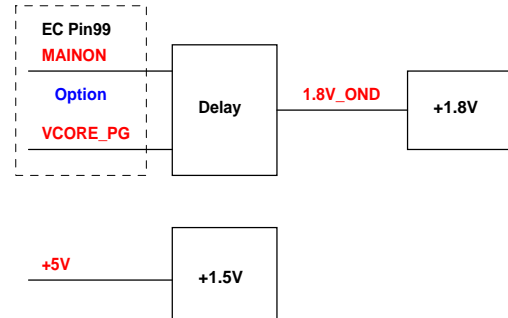
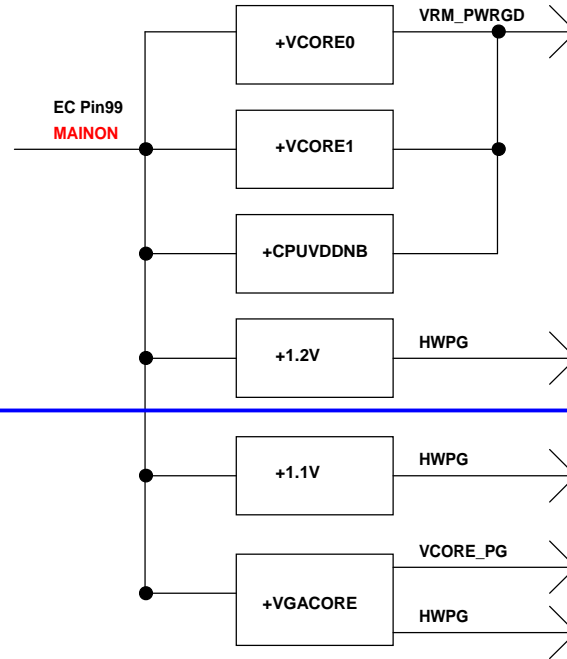




### CPU Power 1



### CPU Power 2



**PROJECT : AX2/7**  
Quanta Computer Inc.

Size Custom	Document Number <b>Power control</b>	Rev 3A
Date: Thursday, December 24, 2009	Sheet 41 of 42	

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLAVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER ( 3_3V )	

## SMBUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

## PCB STACK UP

LAYER 1 : TOP  
LAYER 2 : GND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : VCC  
LAYER 6 : BOT

## PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
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**PROJECT : AX2/7**  
Quanta Computer Inc.

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